CLAIMS

What is claimed is:

1. A semiconductor device including a processor having reprogrammable instructions implemented in field-programmable logic, where all I/O connections for said field-programmable logic connect to said DSP processor.

2. A family of two or more ASIC devices including a processor having mask-programmable instructions implemented in ASIC logic, each device member of said family having different amounts of ASIC logic available, and each member of said device family having substantially identical processors, processor memory, and numbers of I/O.

3. The device family of ASIC devices of claim 2 where all members of said family can plug into the same socket in a target system and function properly.

4. A method for implementing DSP software functionality in a device containing a processor and field-programmable logic, comprising:

performance-profiling the execution of said DSP software functionality to identify the subroutine that dominates the overall execution time ; and

automatically converting, by computer means, the subroutine that dominates the overall execution time into field programmable logic functionality, such that the field programmable logic implementation of said subroutine is implemented in synchronous logic.

5. The method of claim 4 where said the field programmable logic implementation of said subroutine is implemented in logic that is synchronous with the clocks of said DSP processor.

6. The method of claim 4 where said dominant subroutine is implemented in mask-programmed ASIC logic.

7. A method for implementing DSP software functionality in a prototype device containing a processor and field-programmable logic and a production device containing mask-programmed ASIC logic functionality, comprising:

performance-profiling the execution of said DSP software functionality to identify the subroutine that dominates the overall execution time; and

converting the subroutine that dominates the overall execution time into field-programmable logic functionality; and

evaluating the device size and speed required for implementation in a production device where the function implemented in said field-programmable logic functionality is instead implemented using mask-programmed ASIC logic functionality.